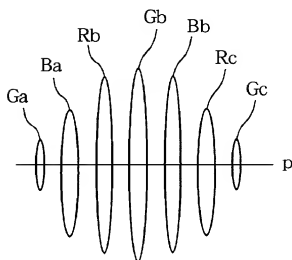


FIG. 1

PRIOR ART

**FIG. 2**

PRIOR ART

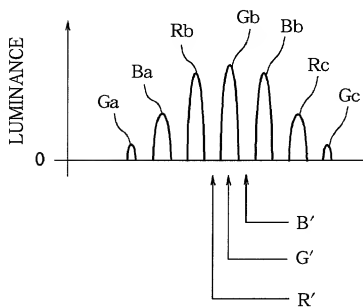
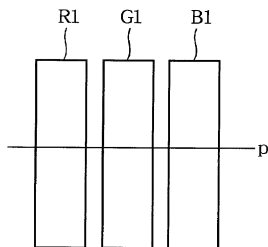


FIG.3

PRIOR ART

**FIG.4**

PRIOR ART

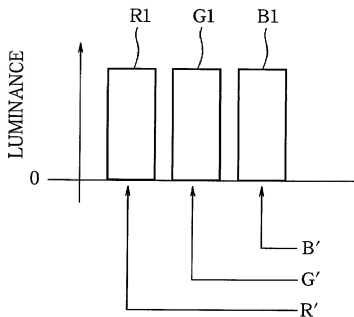


FIG. 5

PRIOR ART

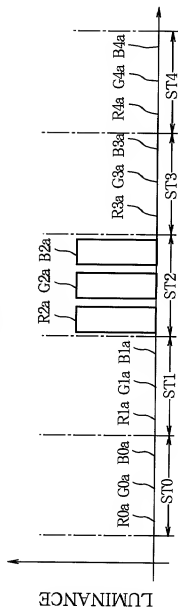


FIG. 6

PRIOR ART

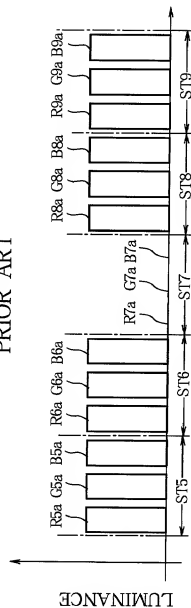


FIG. 7

PRIOR ART

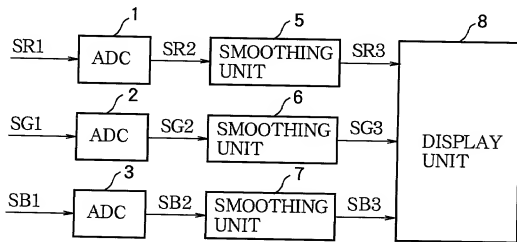


FIG. 8

PRIOR ART

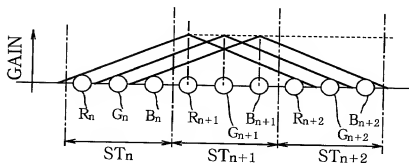


FIG.9
PRIOR ART

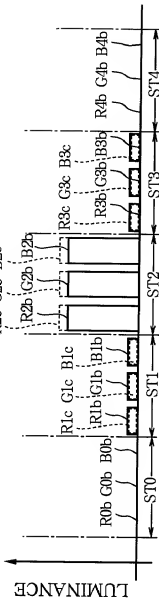


FIG.10
PRIOR ART

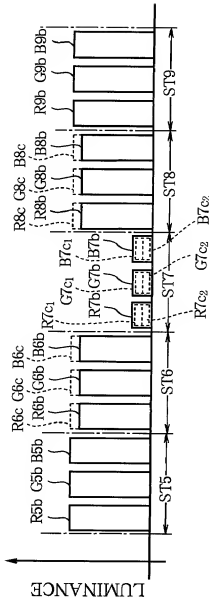
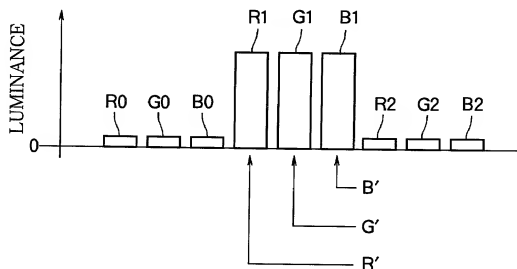
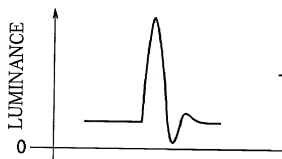


FIG. 11

PRIOR ART

**FIG. 12**

PRIOR ART

**FIG. 13**

PRIOR ART

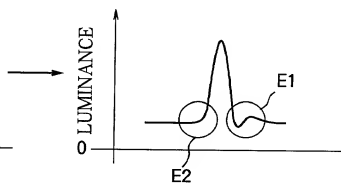


FIG.14

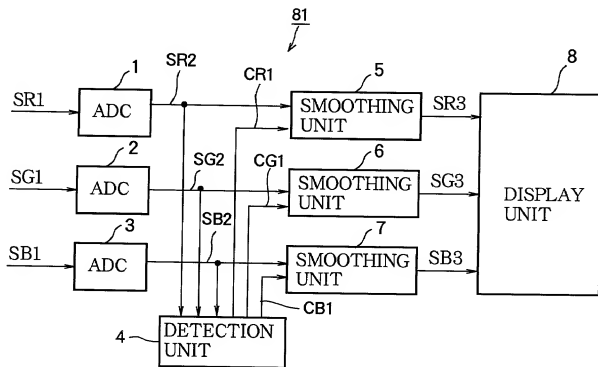


FIG. 15

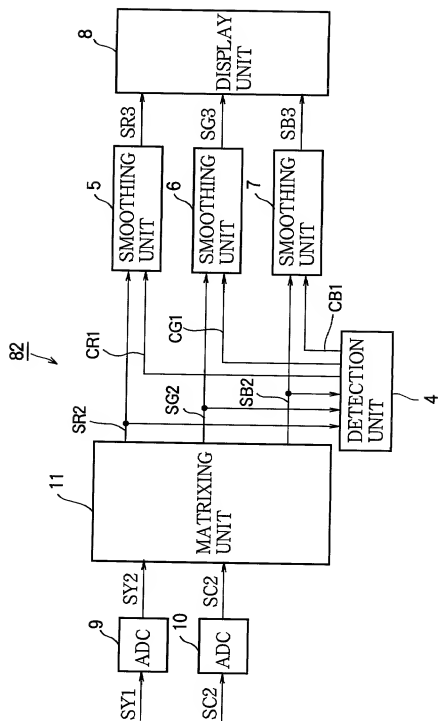


FIG.16

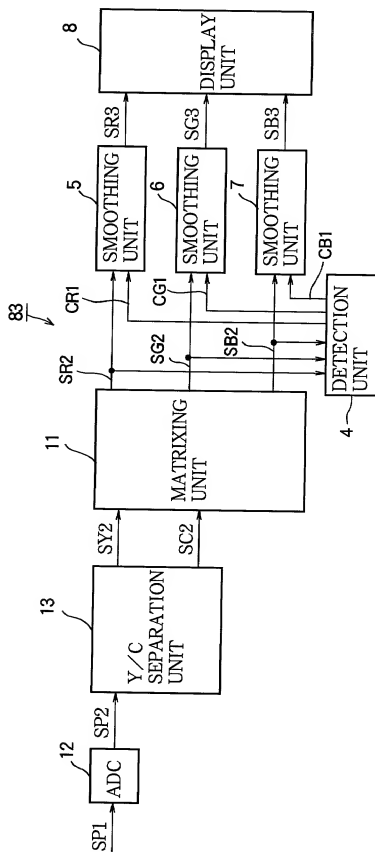


FIG. 17

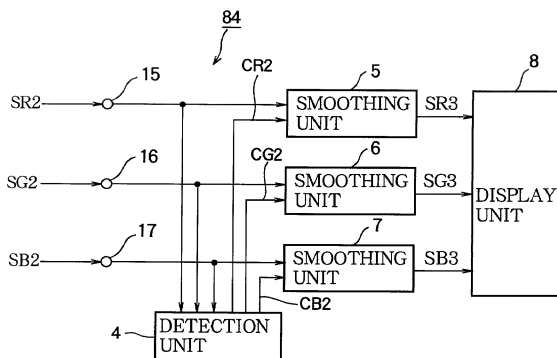


FIG. 18

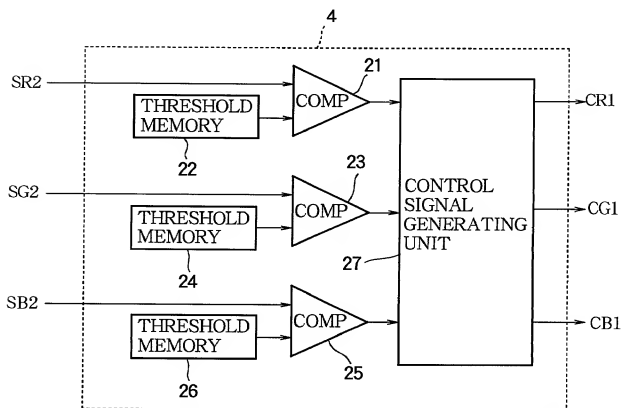


FIG. 19

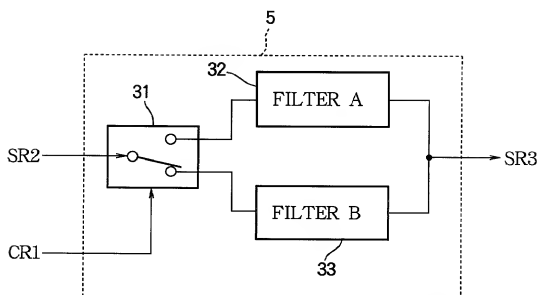


FIG.20

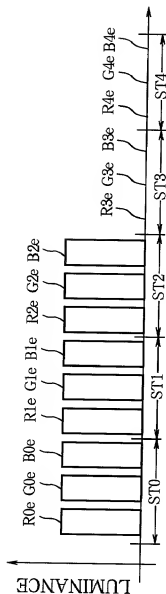


FIG.21

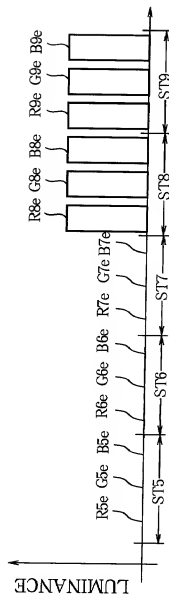


FIG.22

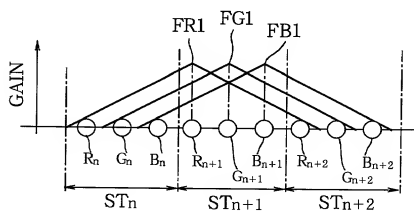


FIG.23

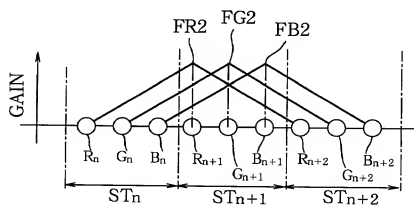


FIG.24

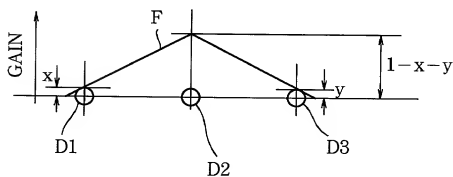


FIG.25

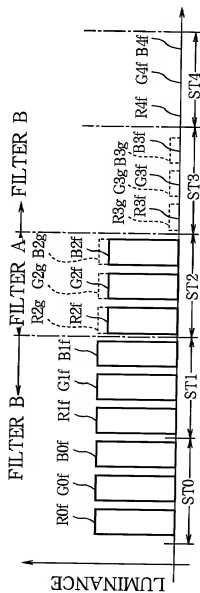


FIG.26

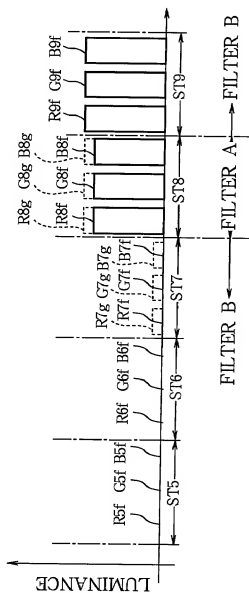


FIG. 27

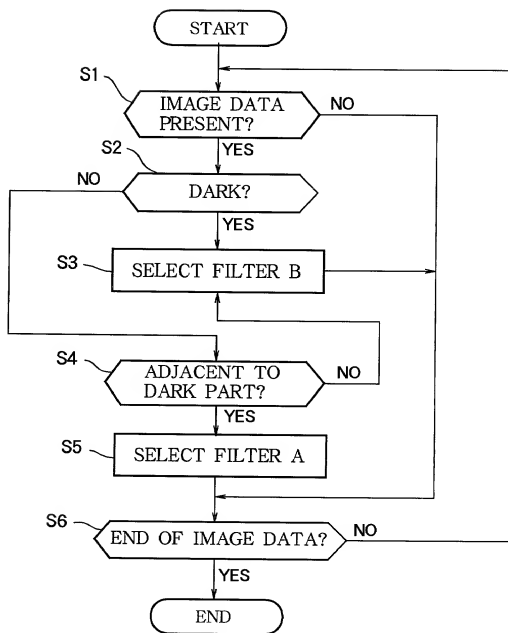


FIG. 28

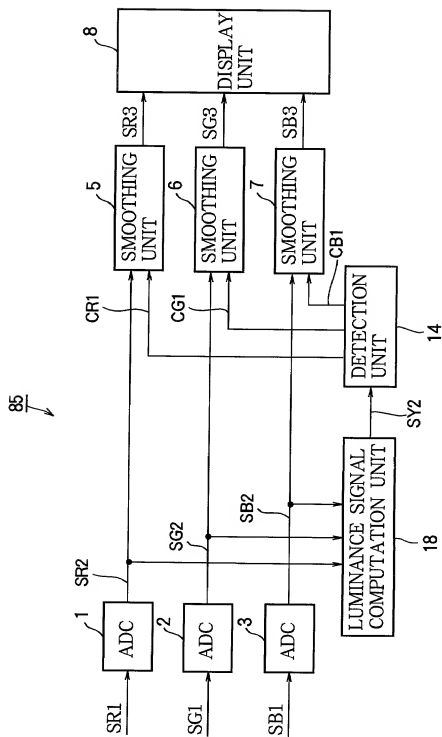


FIG. 29

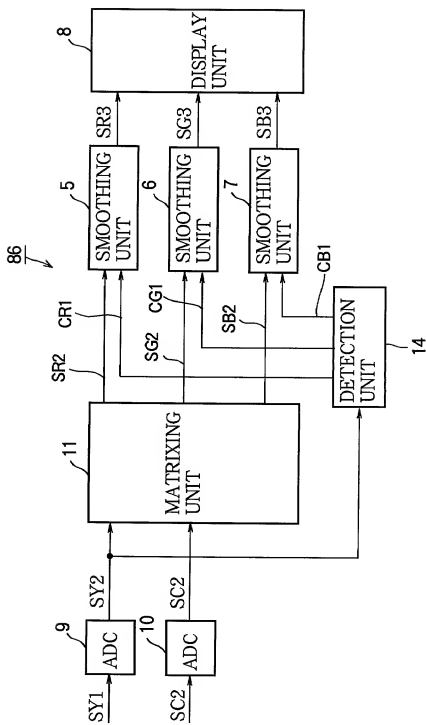


FIG. 30

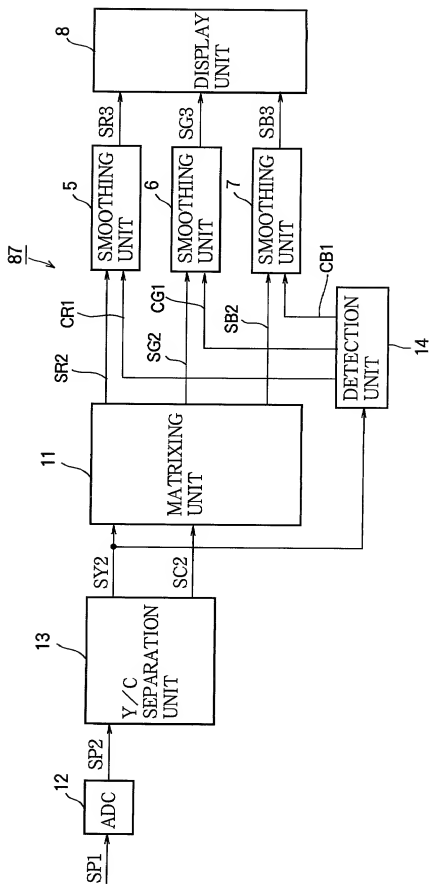
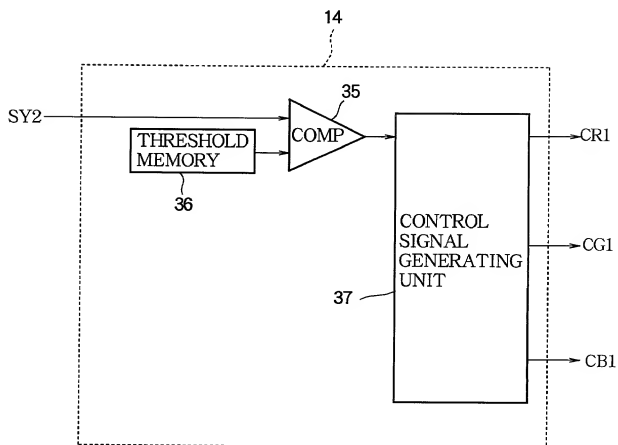


FIG.31



The diagram illustrates a control signal generating unit 24, which is a dashed rectangular block. It has three input lines on the left: SR2, SG2, and SB2. Each input line branches into two parallel paths. For SR2, the paths go through threshold memory 42 and differentiator 43, then comparators 41 and 44. For SG2, the paths go through threshold memory 47 and differentiator 48, then comparators 46 and 49. For SB2, the paths go through threshold memory 52 and differentiator 53, then comparators 51 and 54. The outputs of comparators 41, 44, 46, 49, 51, and 54 are all connected to a large vertical block on the right labeled 56, which is the control signal generating unit.

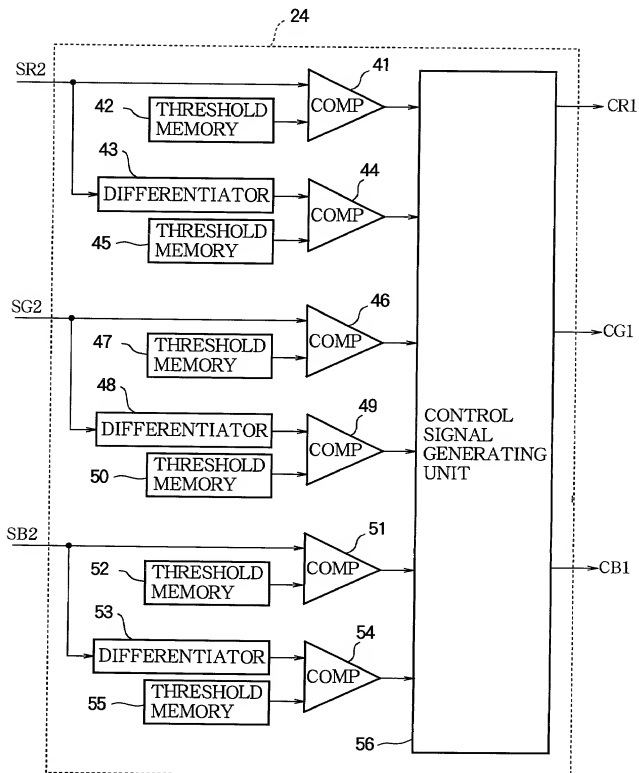


FIG.33

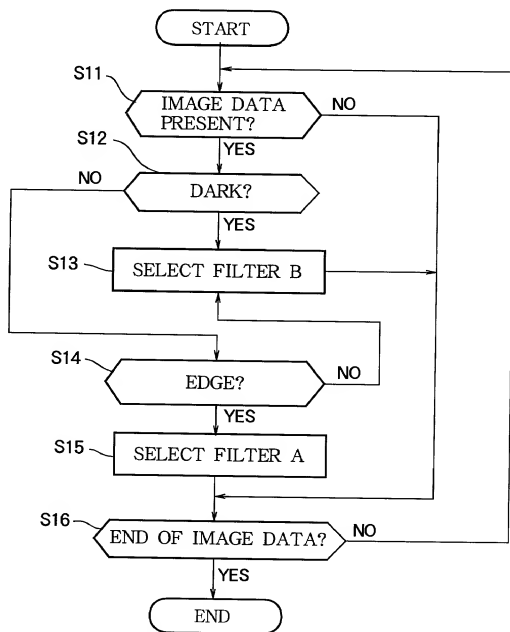


FIG. 34

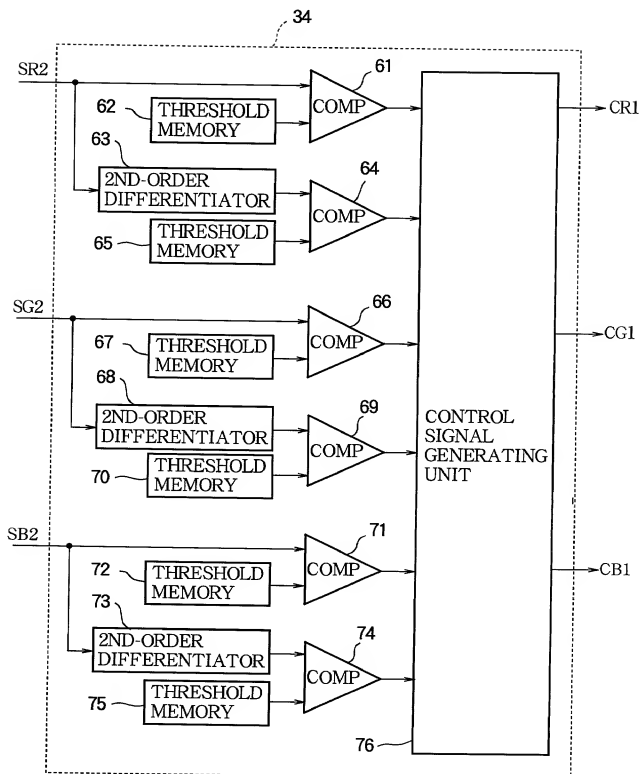


FIG.35

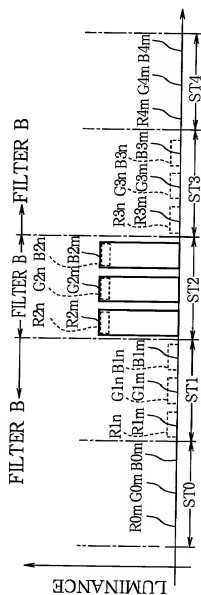


FIG.36

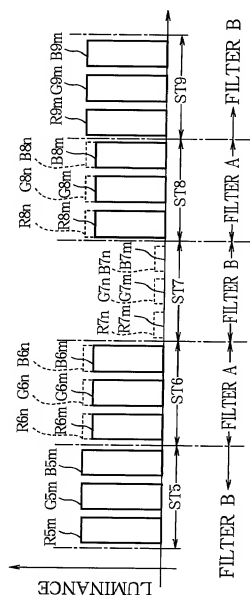


FIG.37

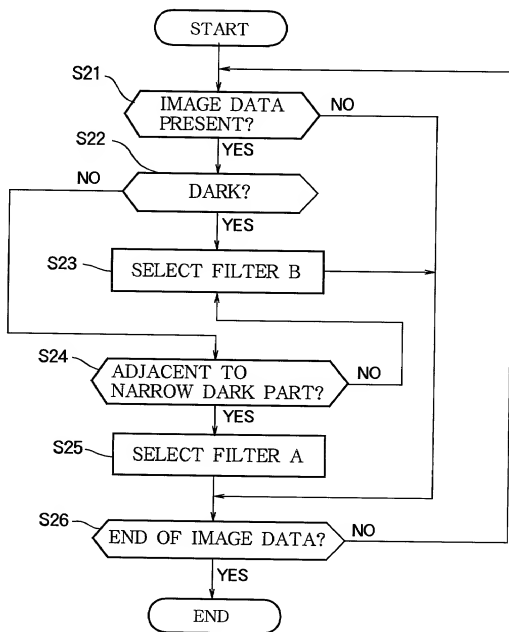


FIG.38

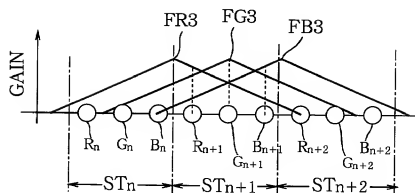


FIG.39

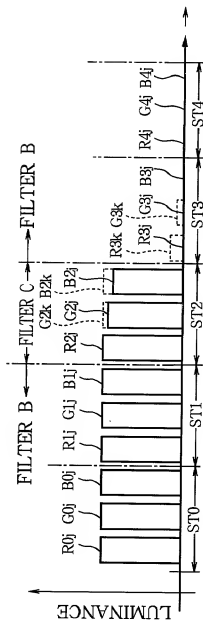


FIG.40

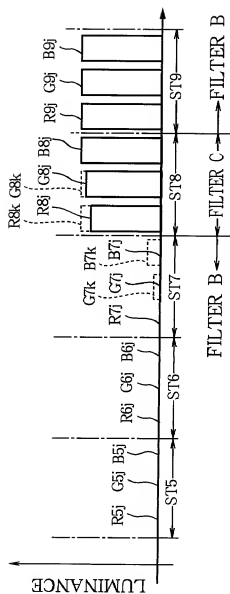


FIG.41

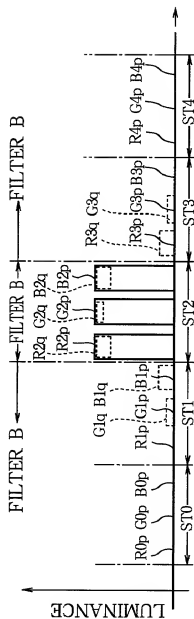


FIG.42

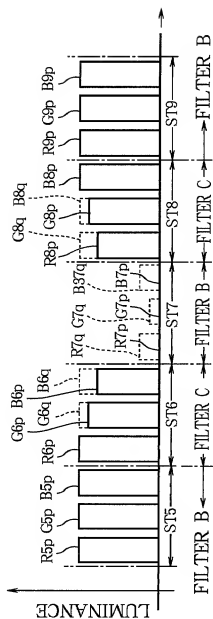


FIG. 43

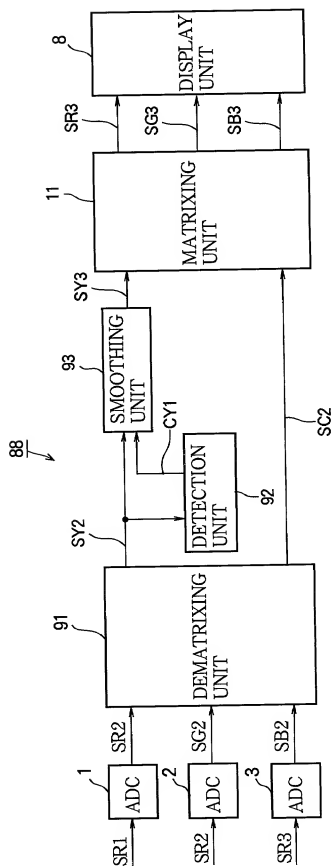


FIG. 44

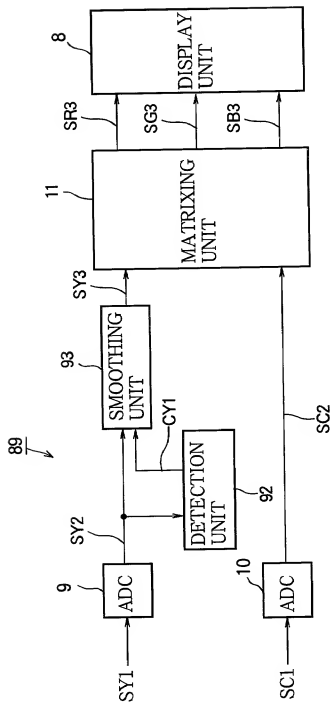


FIG. 45

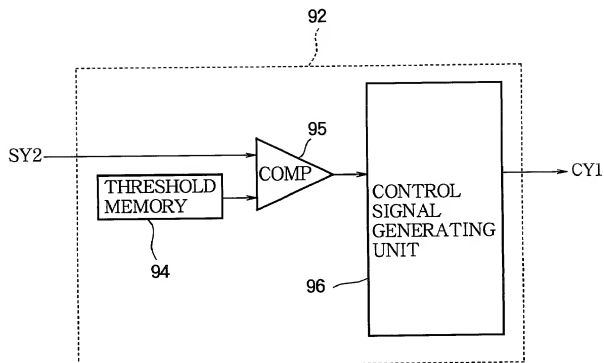


FIG. 46

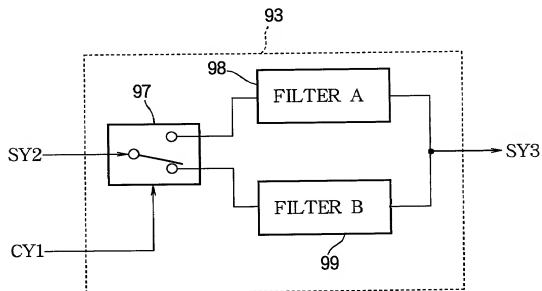


FIG.47

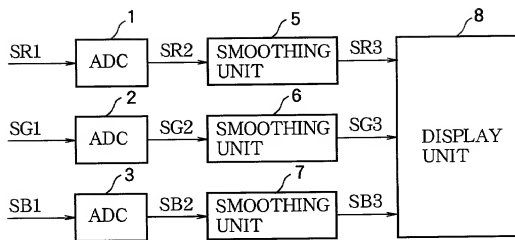


FIG.48

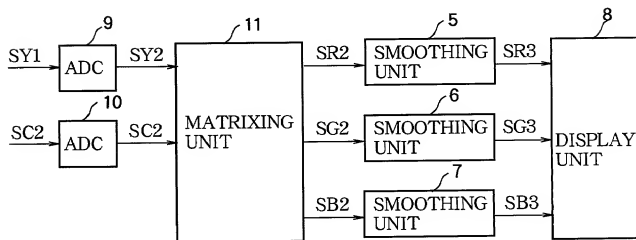


FIG. 49

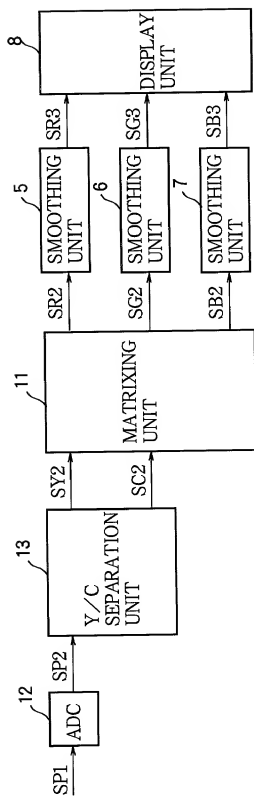


FIG. 50

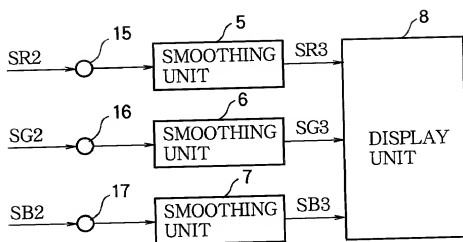


FIG. 51

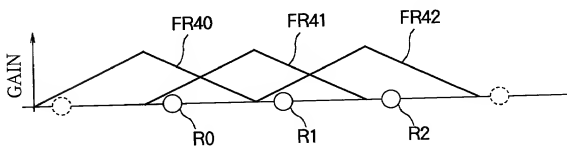


FIG. 52

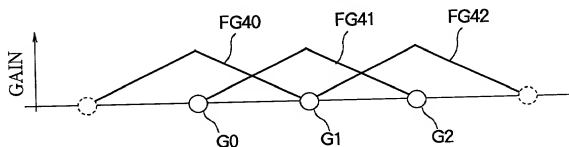


FIG. 53

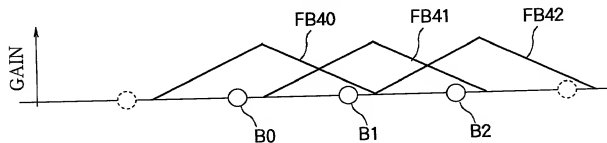


FIG.54

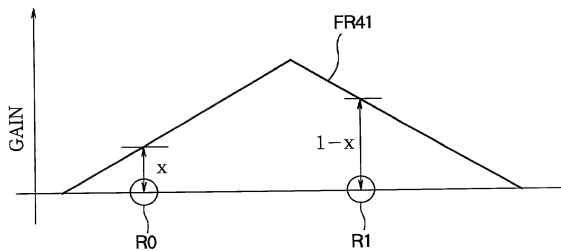


FIG.55

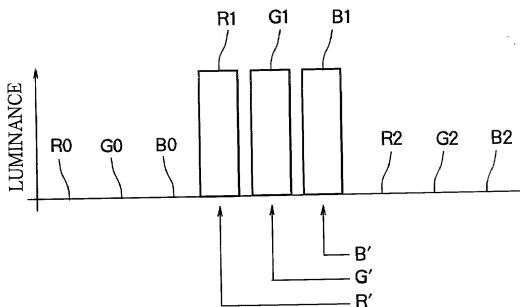


FIG.56

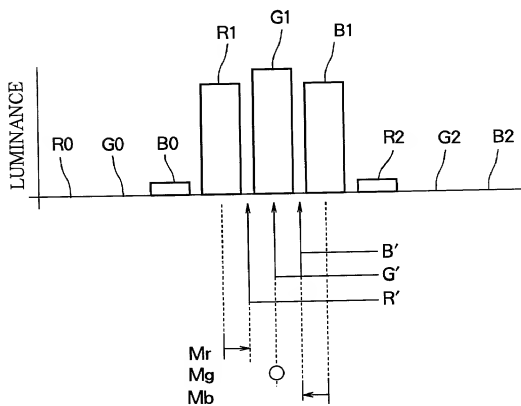


FIG.57

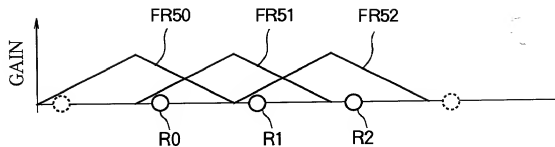


FIG.58

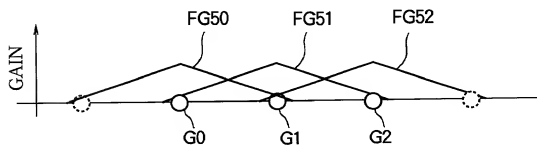


FIG.59

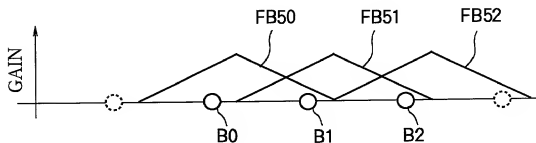


FIG.60

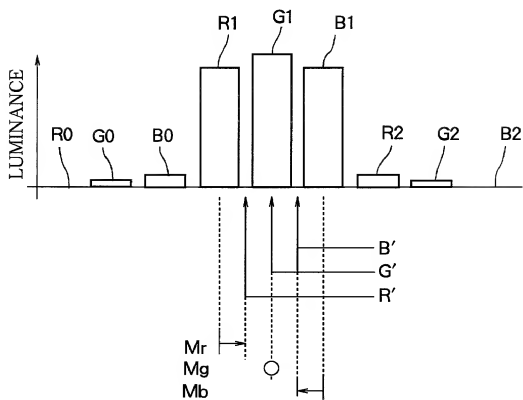


FIG.61

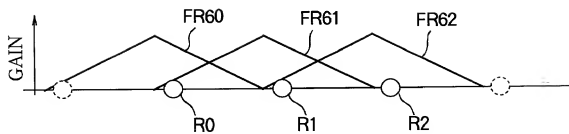


FIG.62

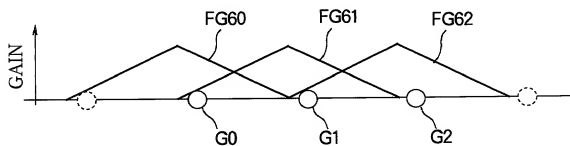


FIG.63

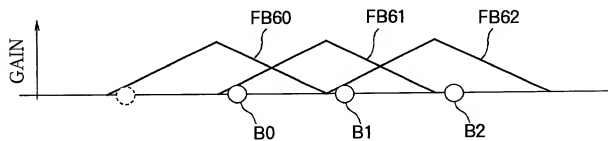


FIG.64

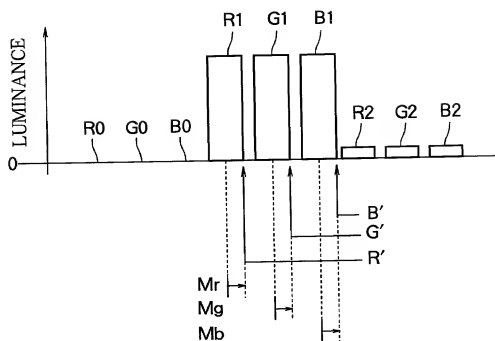


FIG.65

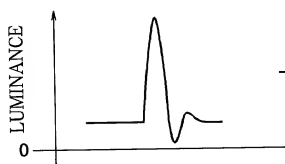


FIG.66

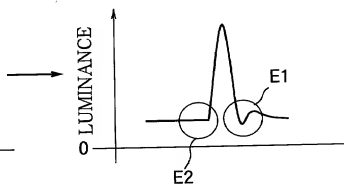


FIG.67

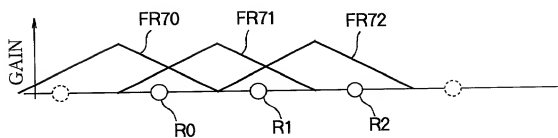


FIG.68

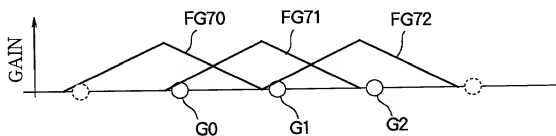


FIG.69

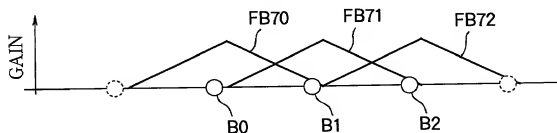


FIG.70

